Linear SuperCapacitor Charger IC With Cell Balancing

CN3125

General Description:

The CN3125 is a complete constant-current /constant voltage linear charger IC to charge single cell or 2-cell superCapacitors from a power supply of 2.7V to 6V. The device contains an on-chip power MOSFET and eliminates the need for the external sense resistor and blocking diode. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The regulation voltage is externally set by a resistor divider. The charge current can be set externally with a single resistor. An internal active balancing circuit maintains equal voltages across each supercapacitor. When the input supply is removed, the CN3125 automatically enters a low power sleep mode, dropping the supercapacitor current to less than 3uA.

Other features include chip enable, undervoltage lockout and supercapacitor power good indicator. The CN3125 is available in a thermally enhanced 8-pin SOP package.

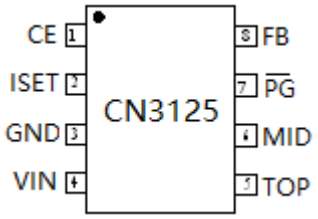
Applications:

- Electric Meter
- SuperCap Backup Circuit
- PC Card, USB Modems
- Portable Equipments

Features:

- Operating Voltage Range: 2.7V to 6V
- On-chip Power MOSFET
- No external Blocking Diode or Current Sense Resistors Required
- Constant Voltage is set by External Resistors
- Charge Current is set by an external resistor
- Continuous Charge Current Up to 1.5A
- Automatic Cell Balancing to Prevent Suercapacitors Overvoltage During Charging
- Constant-Current/Constant-Voltage Operation with Thermal Regulation to Maximize Charge Rate Without Risk of Overheating
- Automatic Low-Power Sleep Mode When Input Supply Voltage is Removed
- Indication for Supercapacitor Power Good
- Chip Enable
- Available in eSOP8 Package
- Pb-free, rohs-Compliant and Halogen Free

Pin Assignment



Typical Application Circuit

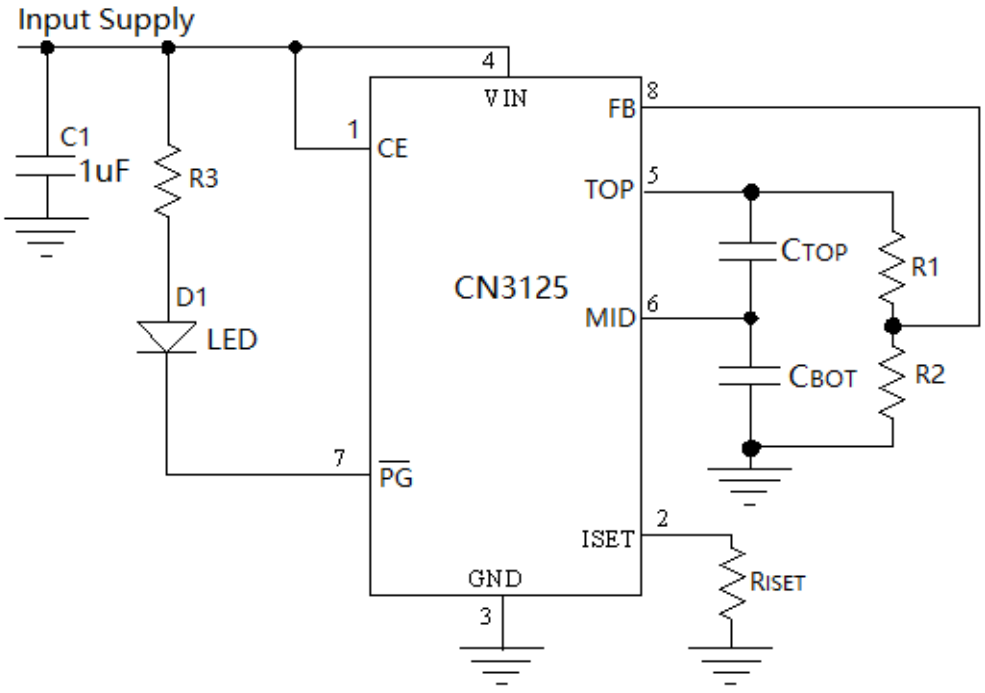


Figure 1 Typical Application Circuit(Charge 2 series-connected Supercapacitors)

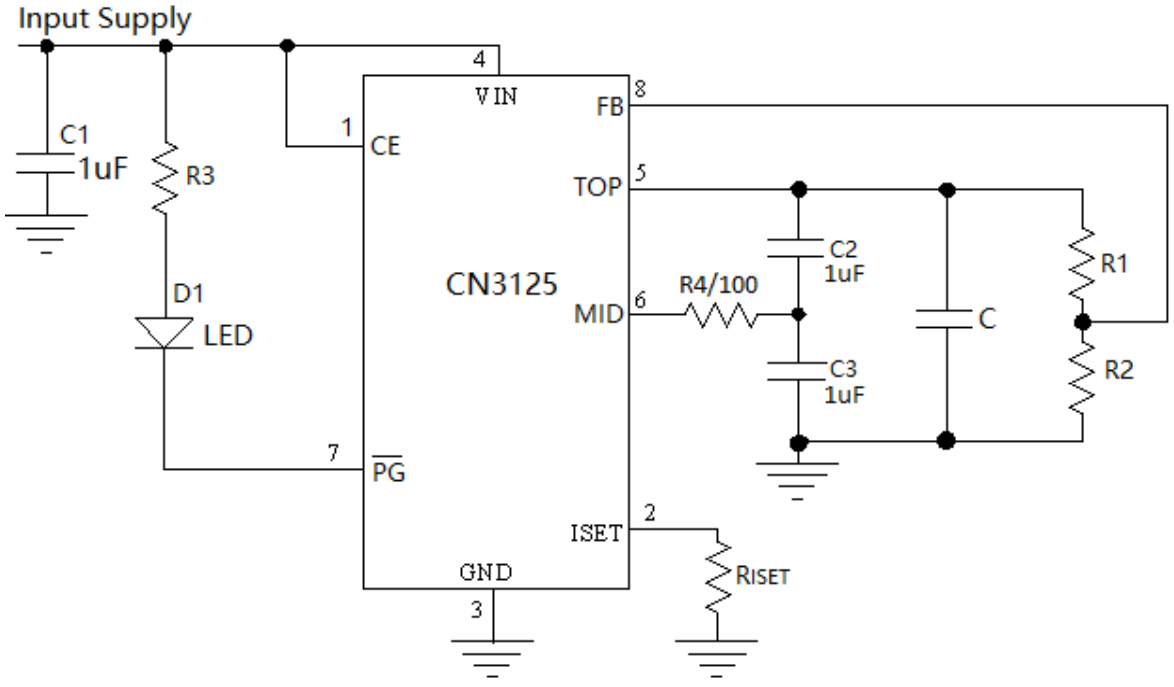


Figure 2 Application Circuit(Charge Single-cell Supercapacitor)

In Figure 1 and 2,

- R3 is for LED current limiting and should be chosen based on LED brightness.
- R4 can be 100 ohm with the size of 0603 or 0402.
- C2 and C3 are 1uF with the size of 0603, respectively.
- For the other components selection, please refer to the section of Application Information in this Datasheet.

Ordering Information：

Part No.	Package	Shipping	Operating Temperature Range
CN3125	eSOP8	Tape and Reel, 4000/Reel	－40℃ to ＋85℃

Block Diagram

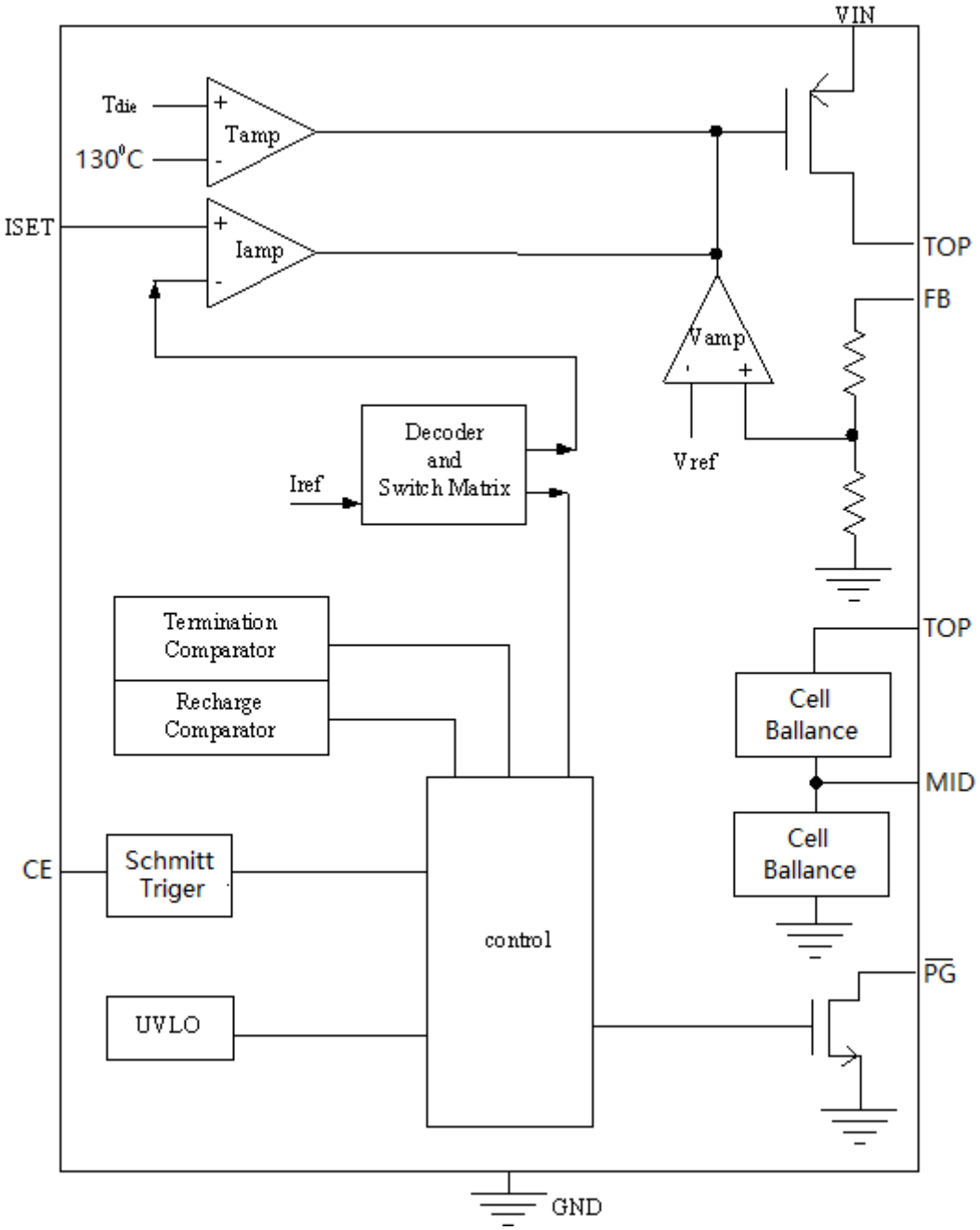


Figure 3 Block Diagram

Pin Description

Pin No.	Name	Function Description
1	CE	**Chip Enable Pin.** A high input will put the device in the normal operating mode. Pulling the CE pin to low level will put the CN3125 into disable mode. When disabled, the whole device is turned off. The CE pin can be driven by TTL or CMOS logic level.
2	ISET	**Constant Charge Current Setting and Charge Current Monitor Pin.** The charge current is set by connecting a resistor R_{ISET} from this pin to GND. When in constant current charge mode, the ISET pin's voltage is regulated to 1.205V. In all modes during charging, the voltage on ISET pin can be used to measure the charge current as follows: $I_{CH} = (V_{ISET} / R_{ISET}) \times 986$
3	GND	**Ground Terminal (Ground).**
4	VIN	**Positive Input Supply Voltage.** V_{IN} is the power supply to the internal circuit. When VIN drops to within 10mv of the TOP pin voltage, CN3125 enters low power sleep mode, dropping TOP and MID pins' current to less than 3uA.
5	TOP	**The Positive Terminal Connection Pin of Top Supercapacitor.** The charge current is delivered from this pin to supercapacitors. If two supercapacitors are charged, the top one's positive terminal should be connected to TOP pin; If only one supercapacitor is charged, then it is tied between TOP pin and GND.
6	MID	**The Connection Pin for the Middle of the 2 Supercapacitors.** The negtive terminal of the top supercapacitor is connected to this pin, and also the positive terminal of the bottom supercapacitor is connected to this pin.
7	$\overline{PG}$	**Open Drain Power Good Output.** When the supercapacitors' voltage rises above 94.1% of the final regulation voltage set by the external resistor divider, this pin becomes low to indicate that the supercapacitor is ready to provide power. When the supercapacitors' voltage falls below 90% of the regulation voltage, the $\overline{PG}$ pin outputs high impedance. When CN3125 is disabled or in sleep mode, $\overline{PG}$ pin outputs high impedance.
8	FB	**Supercapacitor Voltage Feedback Pin.**The regulation voltage in constant voltage mode is set by an external resistor divider connected at FB pin.
9	Exposed PAD	**Soldered to GND.**

Absolute Maximum Ratings

All Terminal Voltage……－0.3V to 6.5V
TOP Short-Circuit Duration……...Continuous
MID Short-Circuit Duration……...Continuous
Thermal Resistance (eSOP8)……TBD

Maximum Junction Temperature……....150℃
Operating Temperature……....－40℃ to 85℃
Storage Temperature….....－65℃ to 150℃
Lead Temperature(Soldering, 10s)…….....260℃

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Electrical Characteristics

(VIN=5V, T_A=－40℃ to 85℃, Typical Values are measured at T_A=25℃,unless otherwise noted)

Parameters	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Supply Voltage	VIN			2.7		6.0	V
Operating Current	I_{VIN}	V_{CE}=5.0V, Normal operation		370	470	570	uA
Sleep Mode Current	I_{SLP}	Sleep mode, VIN current		1.5	2.95	4.4	uA
Shutdown Current	I_{off}	V_{CE}=0V, Measure VIN current		1.5	2.95	4.4	uA
Undervoltage Lockout	Vuvlo	VIN falling			2.4	2.65	V
Undervoltage Lockout Hysteresis	Huvlo				0.12		V
Soft Start Time	t_{SS}			200	320	440	uS
FB Regulation Voltage	V_{REGFB}	Constant Voltage Mode		1.193	1.205	1.217	V
FB Leakage Current	I_{FB}			－100		100	nA
TOP pin Current	I_{CC}	R_{ISET}=1.18K, V_{FB}＝1.0V		900	1000	1100	mA
	I_{LEAK}	Sleep mode or Disabled V_{CE}=low				3	uA
Power Good Threshold	V_{PG}	Voltage at pin FB rises		91.6%	94.1%	96.6%	V_{REGFB}
		Voltage at pin FB falls		87.5%	90%	92.5%	
Maximum Junction Temperature	T_{JMAX}	Constant Temperature Mode			130		℃
Cell-Balancing Shunt Current	I_{SHTOP}	Shunt current from TOP to MID	V_{TOP}=3V	13	18	26	mA
			V_{TOP}=5V	40	55	77	
	I_{SHBOT}	Shunt current from MID to GND	VIN=3V V_{MID}=2V	13	18	26	
			VIN=5V V_{MID}=4V	36	50	70	
Drop Out Voltage	V_{DROP}	Measure (VIN－V_{TOP}) @0.5A			0.28		V
		Measure (VIN－V_{TOP}) @1A			0.45		
		Measure (VIN－V_{TOP}) @1.5A			0.68		
Sleep Mode							
Sleep Mode Threshold	V_{SLP}	V_{IN} from high to low, measures the voltage (V_{IN}－V_{TOP})			10		mV
Sleep mode Release Threshold	V_{SLPR}	V_{IN} from low to high, measures the voltage (V_{IN}－V_{TOP})			60		mV
ISET Pin							
ISET Pin Voltage	V_{ISET}	Constant current mode		1.183	1.205	1.227	V
CE PIN							
Logic Input Low	V_{CEL}	CE voltage falling, Chip disabled				0.7	V
Logic Input High	V_{CEH}	CE voltage rising, Chip enabled		2.2			V
CE input Current	I_{CEL}	CE=GND, VIN=6V		－1			uA
	I_{CEH}	CE=VIN=6V				1	
$\overline{PG}$ **Pin**							
$\overline{PG}$ Sink Current	I_{PG1}	V_{PG}=0.3V, V_{FB}>V_{FBREG}×97%			10		mA
$\overline{PG}$ Leakage Current	I_{PG2}	V_{PG}=6V, V_{FB}≤V_{FBREG}×87%				1	uA

Detailed Description

The CN3125 is a linear charger IC designed primarily for charging single cell or dual-cell supercapacitors. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage to charge the supercapacitors without the need of the external blocking diode and sense resistor. Continuous charge current can be set up to 1.5A with an external resistor. The supercapacitor's final regulation voltage or the constant voltage is also set by an external resistor divider at FB pin, the on-chip reference voltage and error amplifier provide regulation voltage at pin FB with 1% accuracy which can meet the requirement of supercapacitors. The internal thermal regulation circuit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 130℃. This feature protects the CN3125 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the CN3125 or the external components. Another benefit of adopting thermal regulation is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The charge cycle begins when the voltage at the VIN pin rises above the UVLO level and above the voltage at TOP pin, a current set resistor is connected from the ISET pin to ground. At the beginning of the charge cycle, the charger charges the supercapacitors with a constant-current, which is named constant-current mode. When the battery approaches the regulation voltage, the charge current begins to decrease as the CN3125 enters the constant-voltage mode, and the CN3125 will remain in constant-voltage mode as long as the input supply is present.

The open-drain output $\overline{PG}$ indicates if the supercapacitor voltage has approached its final regulation value. The $\overline{PG}$ will remain in high impedance state until the voltage at pin TOP rises above 94.1% of its final regulation voltage, and become high impedance again if the voltage falls below 90% of its final regulation voltage.

The on-chip automatic cell balancing function is provided to prevent supercapacitors from overvoltage during charging, which eliminates the need of the external balancing resistors.

When the input voltage is not present, the charger goes into a sleep mode, dropping the supecapacitors' drain current to less than 3uA. This greatly reduces the current drain on the supercapacitors and increases the standby time.

The charging profile is shown in Figure 4.

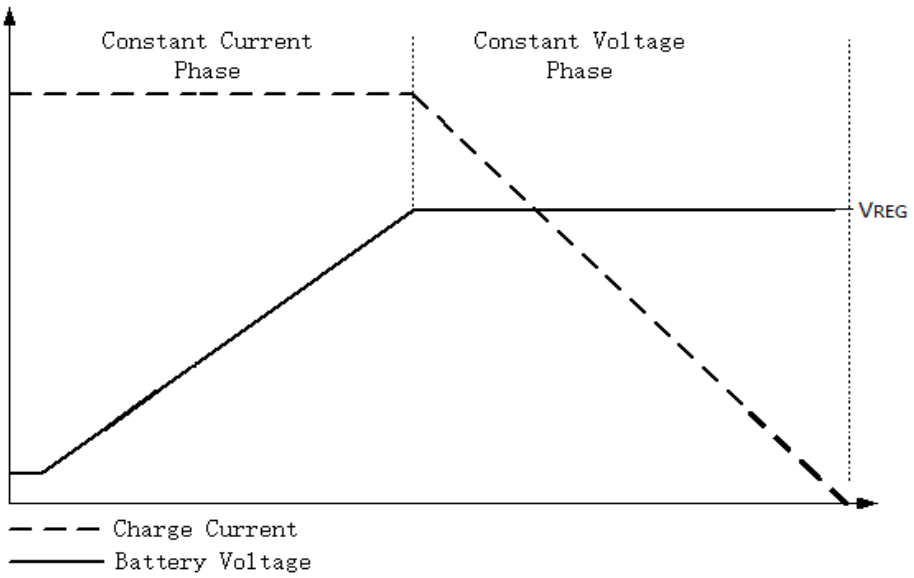


Figure 4 Charging Profile

Application Information

Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until VIN rises above the undervoltage lockout voltage(2.4V typical). The UVLO circuit has a built-in hysteresis of 0.12V.

Chip Enable/Disable

The CN3125 can be disabled by pulling the CE pin to less than 0.7V. For normal operation, pull the CE pin above 2.2V. Applying a voltage between 0.7V to 2.2V to this pin may cause larger operating current, and the CN3125 may be in uncertain state. When the chip is disabled, the internal linear regulator and the power MOSFET are turned off, the device only consumes 1.7uA current from input supply.

Soft-Start

The CN3125 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to full-scale over a period of approximately 320us, this has the effect of minimizing the transient current load on the power supply during start-up.

Sleep mode

There is an on-chip sleep comparator. The comparator keeps the charger in sleep mode if VIN falls below sleep mode threshold(V_{TOP}+10mv). Once in sleep mode, the charger will not come out of sleep mode until VIN rises 60mv(typical) above the voltage at pin TOP.

In sleep mode, the internal circuits are turned off, TOP pin and MID pin's current consumption is less than 3uA.

Setting the regulation voltage in constant voltage mode

The final regulation voltage in constant voltage mode at pin TOP can be set by an external resistor divider at FB pin as shown in Figure 1 and Figure 2, in which resistors R1 and R2 serve the purpose.

The final regulation voltage in constant voltage mode will be given by the following equation:

$$V_{REG} = 1.205 \times (1 + R1 / R2)$$

Where,

V_{REG} is in volt

R1 and R2 are in ohm

R1 and R2's accuracy should be within 1% with the size of 0603 or 0402.

Setting Charge Current

The formula for setting the supercapacitors' charge current in constant current mode is:

$$I_{CH} = 1188V / R_{ISET}$$

Where:

I_{CH} is the charge current in ampere

R_{ISET} is the total resistance from the ISET pin to ground in ohm

For example, if 1000mA charge current is required, calculate:

R_{ISET} = 1188V/1A = 1.18kΩ

For best stability over temperature and time, 1% metal film resistors are recommended. If the charger is in constant-temperature or constant voltage mode, the charge current can be monitored by measuring the voltage at ISET pin, and the charge current is calculated as the following equation:

$$I_{CH} = (V_{ISET} / R_{ISET}) \times 986$$

Constant-Current/Constant-Voltage/Constant-Temperature

The CN3125 use a unique architecture to charge the supercapacitors in a constant-current, constant-voltage, constant temperature fashion as shown in Figure 3. Amplifiers Iamp, Vamp, and Tamp are used in three separate feedback loops to force the charger into constant-current, constant-voltage, or constant-temperature mode,

respectively. In constant current mode the charge current delivered to the capacitors equal to 1188V/R_{ISET}. If the power dissipation of the CN3125 results in the junction temperature approaching 130℃, the amplifier Tamp will begin decreasing the charge current to limit the die temperature to approximately 130℃. As the battery voltage rises, the CN3125 either returns to constant-current mode or it enters constant voltage mode straight from constant-temperature mode.

Automatic Cell Balancing

Due to manufacturing tolerances, capacitance and leakage current can vary from supercapacitor to supercapacitor. Without the automatic cell balancing scheme, the voltages across the supercapacitors could differ from each other and potentially overvoltage a cell. This can affect the performance and lifetime of a supercapacitor.

The CN3125 constantly monitors the voltage difference across both supercapacitors while charging. When the voltage across the supercapacitors is equal, both capacitors are charged with equal currents. If the voltage across one supercapacitor is higher than the other, a voltage-dependent shunt current in parallel with the supercapacitor begins flowing, hence the higher supercapacitor's charge current is decreased. Here the voltage-dependent shunt current means the shunt current is dependent on the input supply voltage, the voltage at TOP pin and MID pin. Since the shunt current is limited, in some cases it can not balance the capacitors' voltage if the leakage currents or capacitances of the two supercapacitors are mismatched largely enough.

When the voltage difference between the 2 supercapacitors is greater than 0.1V, the charge current will be reduced to 10% of the constant current, so it is easier for the cell balancing block to balance the cell voltage. However, since the CN3125 is designed to handle slight mismatch of the supercapacitors, not to correct gross mismatch due to defects. So sometimes there is still risk that the cell voltages can not be balanced due to the capacitors' serious mismatch, if this is the case, the external zener diodes in parallel with the supercapacitors are needed to prevent the supercapacitors from overvoltage.

For example, suppose the constant charge current is 1A, the shunt current of cell balancing is 30mA, then in constant current mode, 3% mismatch can be corrected; When the voltage difference of the 2 supercapacitors is over 0.1V, the charge current will be reduced to 100mA, then about 30% mismatch can be corrected. If the mismatch is over 30%, the external zener diodes in parallel with the supercapacitors are needed, the maximum current flowing through the zener diodes is 10% of the constant current.

Over Current Protection

The CN3125 has built-in over current protection as well as silicon temperature regulation, which will limit the maximum charge current to 1.6A(Typical) in some extreme cases including ISET pin being shorted to GND.

Charging a Single-cell Supercapacitor

The CN3125 can be used to charge single-cell supercapacitor by connecting 2 series-connected capacitors with a capacitance of 1uF from TOP pin to GND and an 100 ohm resistor from MID pin to the middle of the 2 series-connected capacitors as shown in Figure 2, in which resistor R4, capacitor C2 and C3 are for the purpose.

Open-Drain Output $\overline{PG}$

The CN3125 have an open-drain status output $\overline{PG}$ to indicates if the supercapacitors' voltage has approached its final regulation value. When charge cycle starts, the $\overline{PG}$ is in high impedance state, and becomes low if the voltage at pin FB rises above 94.1% of its final regulation voltage, and becomes high impedance again if the voltage falls below 90% of its final regulation voltage.

$\overline{PG}$ pin's being in logic low does not mean the charging is terminated, as a matter of fact the charging is ongoing until the supercapacitors are fully charged.

The pin $\overline{PG}$ is in high impedance state if pin CE is low or the CN3125 is in sleep mode.

The pin $\overline{PG}$ is open drain output, so a pull-up resistor is needed for a certain state, and should be tied to ground if not used.

VIN Bypass Capacitor

Many types of capacitors can be used for input bypassing(C1 in Figure 1 and 2), Generally, a 1uF ceramic capacitor, placed in close proximity to VIN and GND pins, works well. In some applications depending on the power supply characteristics and cable length, it may be necessary to increase the capacitor's value.

The ceramic input capacitor's size should be 0805 or larger.

If the ceramic capacitor is used as the input supply bypassing purpose, a voltage spike may be created when the input voltage is applied to the CN3125 via a cable. If the cable is a bit long, the circuit shown in Figure 5 or a TVS diode from VIN pin to GND should be considered to prevent the CN3125 from being damaged by the voltage spike. Diode D2 in Figure 5 is for the purpose.

For the consideration of the bypass capacitor, please refer to the Application Note AN102 from our website.

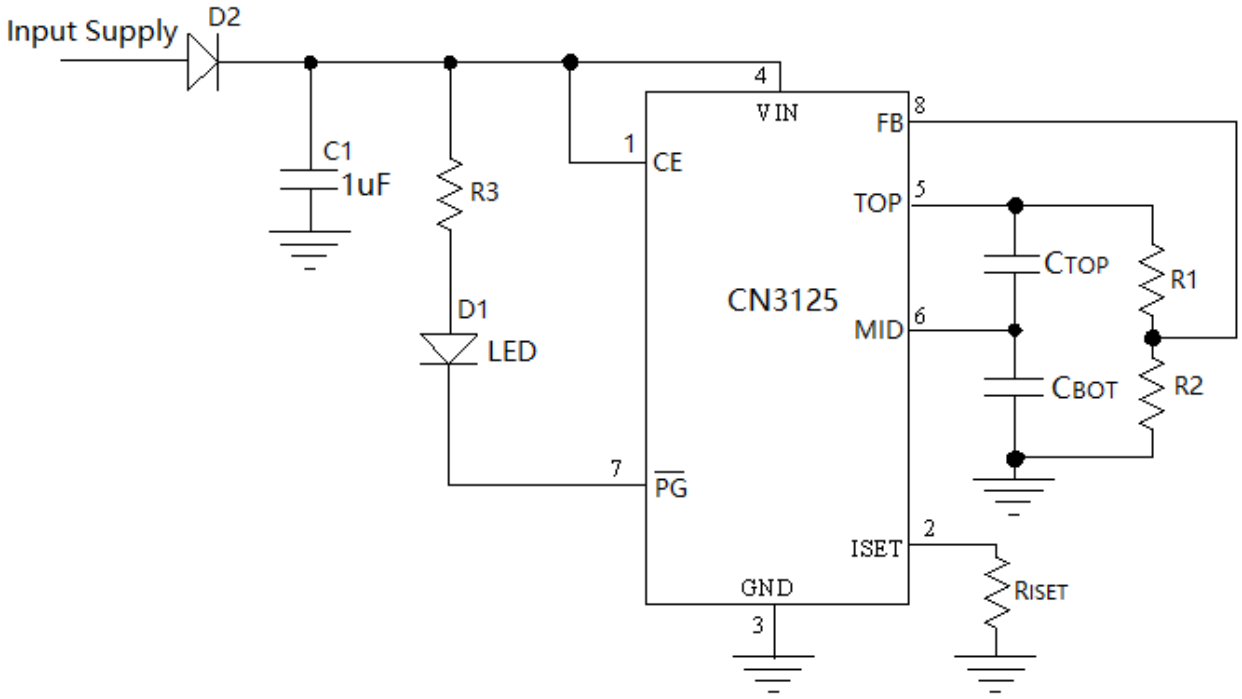


Figure 5 Adding Diode D2 to Suppress Voltage Spike

Stability

If the supercapacitor is present at pin TOP, there is no need to use additional capacitors between TOP pin to GND to stabilize the feedback loop. In case of supercapacitors' absence, a capacitor from pin TOP to GND is needed, generally the feedback loop is stable with an 1uF to 22uF ceramic capacitor. If electrolytic capacitor is used, the capacitance can be as high as 100uF.

In constant current mode, the stability is also affected by the impedance at the ISET pin. With no additional capacitance on the ISET pin, the loop is stable with current set resistors values as high as 50KΩ. However, additional capacitance on ISET pin reduces the maximum allowed current set resistor. The pole frequency at ISET pin should be kept above 200KHz. Therefore, if ISET pin is loaded with a capacitance C, the following equation should be used to calculate the maximum resistance value for R_{ISET}:

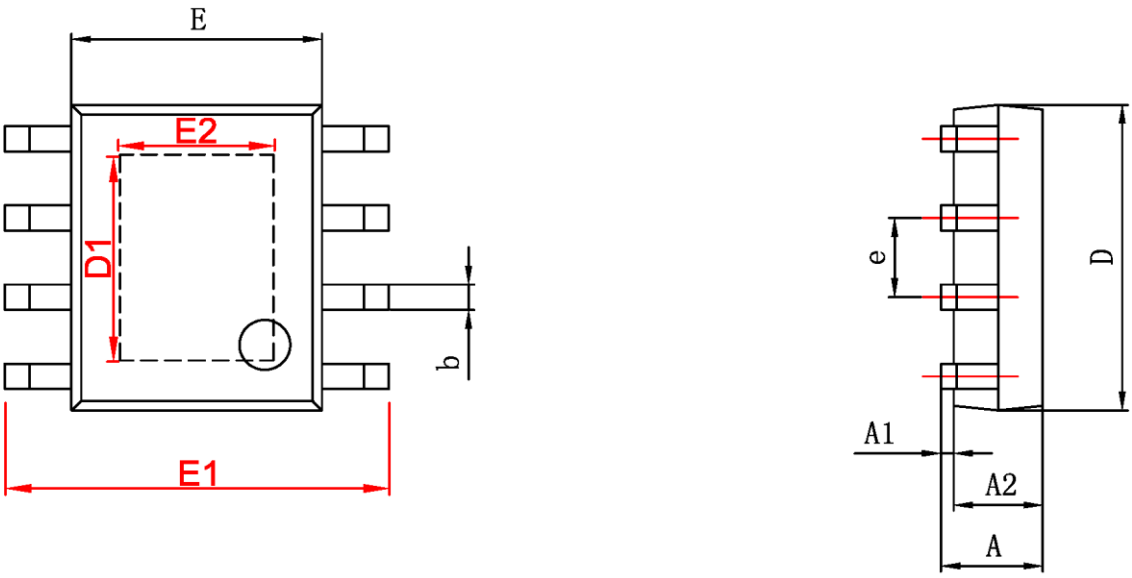
$$R_{ISET} < 1 / (6.28 \times 2 \times 10^5 \times C)$$

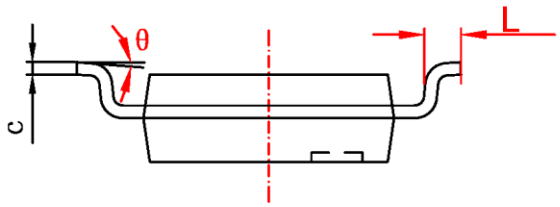
Board Layout Considerations

1. R_{ISET} at ISET pin should be as close to CN3125 as possible, also the parasitic capacitance at ISET pin should be kept as small as possible.
2. The capacitance at VIN pin, TOP pin and MID pin should be as close to CN3125 as possible.
3. It is very important to use a good thermal PC board layout to maximize charging current. The thermal path for the heat generated by the IC is from the die to the copper lead frame through the package lead(especially the ground lead) to the PC board copper, the PC board copper is the heat sink. The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient. Feedthrough vias to inner or backside copper layers are also useful in improving the overall thermal performance of the charger. Other heat sources on the board, not related to the charger, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum charge current.

   The ability to deliver maximum charge current under all conditions require that the exposed metal pad on the back side of the CN3125 package be soldered to the PC board ground. Failure to make the thermal contact between the exposed pad on the backside of the package and the copper board will result in larger thermal resistance.

Package Information





字符	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°